CLAIMS

The claimed invention is:

1. A look-up table (LUT) based logic element (LE), comprising:

m data inputs;

two data outputs;

2k bits of LUT mask,

wherein

the LE includes first and second circuitry configured to accomplish first and second respective identical Boolean functions, each of the first and second circuitry operating on k data inputs responsive to a separate 2k -1 bits of the 2k bits of LUT mask, wherein 2k-m inputs of the m inputs are shared between the first and second circuitry and m-k inputs of each k inputs are independent inputs;

m=k+2;

each of the first and second circuitry includes base circuitry comprising a plurality of multiplexor stages to nominally accomplish a k-1 LUT function operating responsive to the separate 2k -1 bits of the 2k bits of LUT mask;

each of the first and second circuitry further includes an additional stage inserted between a first, earlier, multiplexor stage and a second, later, multiplexor stage of the base circuitry, the additional stage of each of the first and second circuitry configured to selectively pass the outputs from the earlier stage of that circuitry or from the earlier stage of the other circuitry, to the later stage of that circuitry,

the first and second circuitry thereby collectively forming two k input LUT functions with no additional LUT mask bits beyond the 2^k bits of LUT mask; and

the LE further comprises an SRAM-controlled 2:1 mux whose output provides an (m+1)st data input, wherein the 2:1 mux selects between a signal provided at one of the m data inputs and a signal that is not provided at one of the m data inputs.

2. The LE of claim 1, wherein:

the LUT-based LE is within a logic array block (LAB); and

the signal that is not provided at one of the m data inputs is a tap line from the secondary signals for the LAB.

3. The LE of claim 1, wherein:

the LUT-based LE is within a logic array block (LAB); and

the signal that is not provided at one of the m data inputs is a tap line from the general routing resources of the LAB.

4. The LE of claim 1, wherein:

the signal that is not provided at one of the m data inputs is zero or ground.

5. The LE of claim 4, wherein:

the SRAM-controlled 2:1 mux is implemented as an AND gate.

6. The LE of claim 1, wherein the LUT-based LE implements two multiplexer elements of a crossbar or barrel shifter network.

7. The LE of claim 6, wherein:

the shared inputs constitute the data bits two two compatible muxes and the independent inputs constitute distinct select bits to the two compatible muxes.

8. The LE of claim 7, further comprising:

circuitry to transform the select bits to one of the two compatible muxes to effectively rotate the data bits to that one compatible mux to align with the data bits to the other of the two compatible muxes.

9. The LE of claim 2, wherein:

the (m+1)st data input is used to replace a data input to one of the pair of LUT circuits.

10. The LE of claim 3, wherein:

the (m+1)st data input is used to replace a data input to one of the pair of LUT circuits.

11. The LE of claim 4, wherein:

the (m+1)st data input is used to replace a data input to one of the pair of LUT circuits.

12. A method of generating a design configuration for an LE, comprising:
processing design language representing a barrel shifter; and
generating a design configuration for the LE of claim 8.

13. A method of generating a design configuration for an LE, comprising:
processing design language representing a barrel shifter; and
generating a design configuration for the LE of claim 9.

14. A method of generating a design configuration for an LE, comprising:
processing design language representing a barrel shifter, and
generating a design configuration for the LE of claim 10.

15. A method of generating a design configuration for an LE, comprising:
processing design language representing a barrel shifter, and
generating a design configuration for the LE of claim 11.